DETAILED ACTION

1. Claims 2-5, 7-9, 13-16, 18-21, 23-24, 26-28, and 33-41 have been presented for examination. The Request for Continued Examination submitted 10/29/10 has been acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 28, 35, and 38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 35 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted step is: generating a plurality of test designs. Independent claim 33 is directed to a method for generating a plurality of test designs but does not recite the step of generating a plurality of test designs. The step of generating a plurality of test designs is essential to claim 35 which recites applying the plurality of test designs but also fails to recite generating a plurality of test designs

Claim 28 is rejected by virtue of its dependency.

Claim 38 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: a processor configured to generate a plurality of test designs. Independent claim 36 is directed to a computer system for generating a plurality of test designs but does not recite an element configured to generate a plurality of test designs. An element configured to generate a plurality of test designs is essential to claim 38 which recites a processor configured to apply the plurality of test designs but fails to recite generating a plurality of test designs.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in Graham **v.** John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 2, 5, 13, 18-21, 26-27, 33-34, 36-37, 39 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang et al. (U.S. Patent No. 6,269,467) in view of Bening et al. ("Optimizing Multiple EDA Tools within the ASIC Design Flow").**

As per claim 33, Chang is directed to a method of generating a plurality of test designs assoiated with a design automation tool, the method comprising: (a) instantiating an input/output (I/O) structure of a module having input and output pins **(column 41, lines 4-11)**; (b) selecting a plurality of submodules, wherein the plurality of submodules comprises input and output lines **(column 8, lines 12-25)**; (c) parameterizing the plurality of submodules for interconnection with the module **(column 22, lines 53-59)**; (d) interconnecting the lines of the plurality of parameterized submodules based on a selection of a particular type of interconnect from a plurality of interconnect types **(column 23, lines 30-43)**; and (f) connecting the plurality of parameterize submodules to the input and output pins of the module **(column**

24, lines 11-19) but fails to explicitly disclose applying a function to select a plurality of submodules from a design module library.

Bening teaches selecting a plurality of submodules from a design module library **(page 51, column 2, 2nd paragraph)** wherein the said selecting the plurality of submodules is constrained based on a hardware family of the one of the test designs, wherein the hardware family is selected from a plurality of hardware families **(page 51, "Optimizing physical design", instantiating vendor-specific macro cells).** It would have been obvious to an ordinary person skilled in the art to combine the method of generating a plurality of test designs of Chang with the creation of test designs with EDA tools of Bening in order to optimize EDA tools **(Bening, page 46, 1st paragraph)**.

As per claim 2, the combination of Chang and Bening already discloses the method of claim 33, wherein the design automation tool is used to implement hardware descriptor language designs on a programmable chip **(Bening, page 46, 1st column, 2nd paragraph)**.

As per claim 5, the combination of Chang and Bening already discloses the method of claim 33, wherein the design automation tool is a synthesis or a place and route tool **(Bening, page 52, scan chain hookup)**.

As per claim 13, the combination of Chang and Bening already discloses the method of claim 33, wherein parameterizing the plurality of submodules comprises defining interfaces, data width, an the type of signal for one of the input lines and one of the output lines associated with one of the parameterized submodules **(Chang, column 23, line 66 – column 25, line 4)**.

As per claim 34, the combination of Chang and Bening already discloses the method for claim 33, wherein the plurality of interconnect types include an interconnect having a mathematical expression, an interconnect having conditional logic, or a direct interconnect **(column 24, lines 11-29 and lines 45-49 and Figures 36-37)**.

Claims 36, 18, 21 and 37 are directed to a computer system for generating a plurality of test designs associated with a design automation tool, the computer system comprising a memory and processor configured to perform the method steps of claims 33, 2, 5, and 34 and are therefore rejected over the same prior art combination.

As per claim 19, the combination of Chang and Bening already discloses the computer system of claim 36, wherein the design automation tool is used to implement designs on an ASIC (**Chang, column 8, lines 6-14**).

As per claim 20, the combination of Chang and Bening already discloses the computer system of claim 36, wherein the design automation tool is an electronic design automation tool (**Chang, column 8, lines 6-14**).

Claims 39, 26-27 and 41 are directed to an apparatus for generating a plurality of test designs associated with a design automation tool, the apparatus comprising storage and processing means for performing the method steps recited in claims 33, 2, 19, and 34 and are therefore rejected over the same prior art combination.

4. **Claims 4, 7-9, 15-16, and 23-24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (U.S. Patent No. 6,269,467) in view of Bening et al. ("Optimizing Multiple EDA Tools within the ASIC Design Flow") **in further view of Zaidi et al. (U.S. Patent Application Publication 2002/0038401 A1).**

As per claim 4, the combination of Chang and Bening already discloses the method of claim 33, but fails to explicitly disclose wherein instantiation constraints are used to select the plurality of submodules. Zaidi teaches wherein instantiation constraints are used to select the plurality of submodules (**[0085]**). Chang, Bening, and Zaidi are analogous art because they are all from the same field of endeavor, validating an IC. It would have been obvious to one of ordinary skill in the art at the time of

the invention to combine the method of generating a plurality of IC test designs with a testbench of Chang and Bening with the instantiation constraints of Zaidi in order to provide pre-designed SoC architecture to decrease development time **(Zaidi, [0013], [0016])**.

As per claim 7, the combination of Chang and Bening already discloses the method of claim 33, but fails to explicitly disclose identifying a plurality of inputs, wherein the inputs indentified comprise the input pins of the module, one of the output lines of one of the parameterized submodules, and registers. Zaidi teaches identifying a plurality of inputs, wherein the inputs indentified comprise the input pins of the module, one of the output lines of one of the parameterized submodules, and registers (**[0048]-[0060]**). Chang, Bening, and Zaidi are analogous art because they are all from the same field of endeavor, validating an IC. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of generating a plurality of IC test designs with a testbench of Chang and Bening with the interconnecting logic of Zaidi in order to provide pre-designed SoC architecture to decrease development time (**Zaidi, [0013], [0016]**).

As per claim 8, the combination of Chang, Bening, and Zaidi already discloses the method of claim 7, further comprising identifying a plurality of inputs, wherein the outputs identified comprise the output pins of the module, one of the input lines of one of the parameterized submodules, and registers (**Zaidi, [0048]-[0060]**).

As per claim 9, the combination of Chang, Bening, and Zaidi already discloses the method of claim 8, further comprising classifying the inputs and outputs indentified as clock lines, control lines, and data lines (**Bening, page 54, module code, signals q, clk, and d**).

As per claim 15, the combination of Chang, Bening, and Zaidi already discloses the method of claim 9, wherein one of the test designs further comprises a clock structure for one of the outputs (**Zaidi, [0047]**).

As per claim 16, the combination of Chang, Bening, and Zaidi already discloses the method of 15, wherein the clock structure includes a synchronous or an asynchronous structure (**Zaidi, [0047]**).

Claims 23-24 are directed to a computer system (**Chang, column 26, lines 13-50**), comprising: memory operable to hold information associated with a design module library, a processor coupled to memory, the processor configured to execute a method with the same limitations of claim 6-8 and are therefore rejected over the same art combination.

5. Claims 28, 35, 38, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (U.S. Patent No. 6,269,467) in view of Bening et al. ("Optimizing Multiple EDA Tools within the ASIC Design Flow") **in further view of Dustin ("Automated Testing Tools").**

As per claim 35, the combination of Chang and Bening already discloses the method of claim 33 but fails to explicitly disclose determining whether a predetermined number of test designs for testing the design automation tool has been generated; and applying the plurality of test designs to test the design automation tool. Dustin teaches determining whether a predetermined number of test designs for testing the design automation tool has been generated (**page 4, 1st paragraph**); and applying the plurality of test designs to test the design automation tool (**page 4, 1st paragraph, help produce the integration test**). Chang, Bening, and Dustin are analogous art because they are all directed to generating test designs. It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the method of generating a plurality of test designs of Chang and Bening with the determination step of Dustin in order to gain insight into the effectiveness of the test suite (**Dustin, page 4, 1st paragraph**).

As per claim 28, the combination of Chang, Bening and Dustin already discloses the method of claim 35, further comprising selecting a plurality of submodules upon said determining that the predetermined number of the test designs is not generated (**Dustin, page 4, 1st paragraph, help produce the integration test**).

Claim 38 is directed to a computer system configured to perform the method steps of claim 35 and is therefore rejected over the same prior art combination.

Claim 40 is directed to an apparatus with means for performing the method steps of claim 28 and is therefore rejected over the same prior art combination.

6. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (U.S. Patent No. 6,269,467) in view of Bening et al. ("Optimizing Multiple EDA Tools within the ASIC Design Flow") **in further view of Goossens ("Design of Heterogeneous ICs for Mobile and Personal Communication Systems").**

As per claim 14, the combination of Chang and Bening is directed to the method of claim 33, wherein submodules comprise memory and timers **(Chang, column 23, lines 23-29)** but fails to disclose wherein submodules comprise adders and phase lock loops. Goossens teaches submodules comprising of adders and phase lock loops **(page 524-525, Figure 1, Section 3.2)**. Chang, Bening, and Goossens are analogous art because they are all from the same field of endeavor, validating an IC. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of generating a plurality of IC test designs with a testbench of Chang and Bening with the adders and phase lock loops of Goossens in order to allow the design of heterogeneous IC architecture **(page 524, Section 1)**.

7. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (U.S. Patent No. 6,269,467) in view of Bening et al. ("Optimizing Multiple EDA Tools within the ASIC Design Flow") **in further view of Rajsuman (U.S. Patent No. 6,678,645)**.

As per claim 3, the combination of Chang and Bening already discloses the method of claim 33, wherein the plurality of submodules comprises a memory module **(Chang, column 23, lines 23-26)** but fails to explicitly disclose wherein the plurality of submodules comprises a Digital Signal Processor

(DSP) Core. Rajsuman teaches generating a plurality of test designs of an ASIC including DSP and memory submodules **(column 1, lines 16-29)**. Chang, Bening, and Rajsuman are analogous art because they are all from the same field of endeavor, validating an IC. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of generating a plurality of test designs of Chang and Bening with the submodules of Rajsuman in order to verify the entire system the way it would be used by the end user **(Rajsuman, column 3, lines 34-38)**.

Response to Arguments

8. Applicant's arguments filed 10/29/10 have been fully considered but they are not persuasive.

9. Applicant's arguments regarding the amended limitations and new claims have been considered but are moot in view of the new grounds of rejection. Chang teaches the amended limitations "interconnecting the lines of the plurality of parameterized submodules based on a selection of a particular type of interconnect form a plurality of interconnect types" as detailed above in the prior art rejection of Section 3.

As all independent claims remain rejected, all dependent claims remain rejected.

Conclusion

10. The prior art made of record is not relied upon because it is cumulative to the applied rejection. These references include:

1. U.S. Patent No. 6,477,691 B1 issued to Bergamashi/Rab et al. on 11/05/02.

2. U.S. Patent Application Publication No. 2004/0015792 A1 published by Kubista on 01/22/04.

3. U.S. Patent No. 6,053,947 issued to Parson on 04/25/00.

4. "ASIC to FPGA Design Methodology & Guidelines" published by Altera in July 2003.

5. U.S. Patent No. 7,085,702 issued to Hwang et al. on 08/01/06.

6. U.S. Patent Application Publication No. 2004/0210798 A1.

7. U.S. Patent No. 6,907,550 B2 issued to Webser et al. on 06/14/05.

8. U.S. Patent No. 6,378,088 B1 issued to Mongan on 04/23/02.

9. U.S. Patent No. 6,189,116 B1 issued to Mongan et al. on 02/13/01.

10. U.S. Patent No. 6,334,207 issued to Joly et al. on 12/25/01.

11. U.S. Patent No. 5,754,760 issued to Warfield on 05/19/98.

11. All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/SUZANNE LO/
Examiner, Art Unit 2128

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